REMARKS

Claims 9-16 were examined and stand rejected. Applicant amends Claims 9 and 13. Applicant respectfully requests reconsideration of pending Claims 9-16, as amended, in view of at least the following remarks.

I. Claims Rejected Under 35 U.S.C. §112

The Patent Office rejects Claims 9-16 under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In response, Applicant amends Claims 9 and 13 to delete the term "permanently." In addition, Claims 9 and 13 are amended to include the limitation, which is supported in the specification as page 7, lines 3-20, to indicate that the IC package is installed onto a printed circuit board via a surface mount attachment.

Furthermore, Applicant respectfully submits that the amendment of Claims 9 and 13 were necessitated to place the application in condition for allowance and, therefore, do not present new issues requiring a new search. Accordingly, Applicant respectfully submits that the claim amendments of Claims 9 and 13 are proper in response to this Final Office Action. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the §112, first paragraph, rejection of Claims 9-16.

II. Claims Rejected Under 35 U.S.C. §103

The Patent Office objects to Claims 9, 13 and 16 as being unpatentable over U.S. Patent No. 5,443,675 issued to Wensink ("Wensink") in view of U.S. Patent No. 5,410,181 issued to Zollo, et al. ("Zollo"). Applicant respectfully traverses this rejection.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or suggest all the claim limitations. (MPEP §2142) For the reasons provided below, the Examiner has failed to establish a *prima facie* case of obviousness in view of the references of record.

As indicated by the Examiner, Applicant's specification supports a surface mount attachment of the IC package to the printed circuit board. As known to those skilled in the art, a surface mount attachment of an IC package integrated circuit onto a printed circuit board involves the bonding of the integrated circuit package to surface pads of the printed circuit board. The surface mount attachment may include a J lead attachment or a gold wing attachment, wherein either J-type leads or gold wings of the package are directly soldered to the printed circuit board surface.

As indicated in Applicant's Background,

> it is sometimes desirable to test an integrated circuit after the IC is mounted to a printed circuit board. Debugging an individual circuit board after assembly to a printed circuit board presently requires the removal of the package from the board. The package is typically removed by applying heat to the assembly to reflow the soldered joints. Unfortunately, reflowing and removing the package may damage the package leads, particularly packages which have fine pitch lead counts. The reflow process also reduces the integrity of the board. It is also desirable to test integrated circuits while the IC packages are still mounted to the printed circuit board. Finally, assembly tests are particularly desirable for high speed devices that are sensitive to the impedance of the circuit board (page 3, line 10 through page 4, line 1). [Emphasis added.]

In other words, a surface mount attachment, as known to those in the art, involves some sort of soldering attachment of either leads, gold wings or physical connection of the IC package to the printed circuit board via solder balls. However, according to the Examiner, the decapsulation process of an IC taught by Wensink establishes an electrical connection within the integrated circuit to be tested where the attachment of the IC package to a connector board is a surface mount attachment. Applicants respectfully disagrees with the Examiner's contention.

The Examiner finds support for the assertion based on FIG. 1 of Wensink. As illustrated in FIG. 1, a DUT 22 includes J-type leads 28 that contact board 26 and, thus, bring out the electrical connections of DUT 22 outside machine 10. (Col. 4, lines 18-21) Furthermore, clamps 24, clamp DUT 22, connector board 26 and top plate 18 together into a fixed or assembly 30. (Col. 4, lines 21-23) In other words, as illustrated with reference to FIG. 1, the failure of Wensink to attach DUT 22 to connector board via a surface mount requires the use of clamps 24. Otherwise, DUT 22 would not be connected to connector board 26.

Applicant respectfully submits that after careful review of FIG. 1, as well as the specification of Wensink, DUT 22 is not connected to connector board 26 via a surface mount attachment. Namely, J-type leads 28 of DUT 22 are not soldered to connector board 26 in accordance with a traditional surface mount attachment. As is clearly illustrated in FIG. 1, clamps 24 provide the connection between J-type leads 28 of DUT 22 to connector board 26.

Accordingly, Applicant respectfully submits that Wensink fails to teach or suggest receiving of an integrated circuit package installed onto a printed circuit board via a surface mount attachment, as required by Claim 9. As depicted in Wensink's FIG. 1, DUT 22 is simply temporarily connected to connector board 26 during decapsulation testing using clamps 24. Therefore, clamping of a DUT to a board during decapsulation testing does not teach or suggest testing of an IC package after the package is installed onto a PCB via a surface mount attachment, as required by Claim 9.

The Examiner acknowledges Applicant's contention that Wensink fails to teach that the IC package is permanently attached with the connector board of the printed circuit board. Although Applicant has eliminated the term "permanently" from Claim 9, Applicant submits that the features of Claim 9 represent the ability to perform decapsulation of an IC package after the IC package is installed onto a printed circuit board.

The Examiner cites Zollo, which according to the Examiner teaches that typically an IC is mounted to a printed circuit board for making interconnection between the IC

and the circuitry on the printed circuit board. Therefore, it would have been obvious to one skilled in the art at the time of the claimed invention to combine the teachings of Zollo into Wensink for making a permanent connection between the IC and the circuitry on the printed circuit board, as taught by Zollo. Applicant respectfully disagrees with the Examiner's contention.

In fact, Applicant respectfully submits that Wensink teaches away from establishing a surface mount attachment between DUT 22 and connector board 26. The decapsulation machine 10 as taught by Wensink, includes a connector board 26 as part of the machine 10. DUT 22, which is not a component of machine 10, includes a plurality of J-type leads 28 that contact board 26 and, thus, bring out the electrical connections of DUT 22 outside machine 10 during testing. (Col. 4, lines 7-21)

In other words, a surface mount attachment of J-type leads 28 to board 26 would require the reflowing of solder to disconnect the J-type leads 28 from connector board 26 once testing is complete. As a result, Wensink teaches the use of the clamps 24 to provide a temporary connection between J-type leads 28 and board 26 which are easily disconnected by removing clamps 24 once testing is complete. Accordingly, Applicant respectfully submits that one skilled in the art would not surface mount DUT 22 to connector board 26, when connector board 26 is a component of decapsulation machine 10, as taught by Wensink.

Consequently, Applicant respectfully submits that the Examiner fails to establish a *prima facie* obviousness rejection of Claim 9 over Wensink in view of Zollo. Applicant submits that this failure arises due to the fact that Wensink teaches away from a surface mount attachment of a DUT 22 of a decapsulation machine 10 to a connector board 26, using clamps 24, to provide attachment during testing, as depicted in FIG. 1. In other words, decapsulation machine 10, as taught by Wensink, is not designed to perform decapsulation testing of an IC package mounted onto a PCB via a surface mount attachment.

Therefore, for at least the reasons described above, Applicant respectfully submits that Claim 9, as amended, is patentable over the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 9.

Claims 10-12

Claims 10-12 depend from Claim 9 and, therefore, include the patentable claim features of Claim 9, as described above. Consequently Applicant respectfully submits that Claims 10-12 are patentable over the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 10-12.

Claim 13

Claim 13, as amended, includes the following feature which is neither taught by either Wensink, Zollo or the references of record:

> receiving an IC package installed onto a first surface of a printed circuit board (PCB) via a surface mount attachment. [Emphasis added]

As indicated above, Wensink does not teach the receiving of an IC package installed onto a first surface of a PCB via a surface mount attachment. As depicted in Wensink's FIG. 1, a DUT 22 is received which includes J-type leads 28. The J-type leads 28 enable connection of the DUT 22 to a connector board 26 of a decapsulation machine 10. However, instead of surface mounting the DUT 22 to connector board 26, the J-type leads contact the connector board 26 by clamping DUT 22 to connector board 26 with clamps 24. In contrast, a surface mount attachment, as required by Claim 13, would require soldering of the J-type leads 28 to the connector board 26.

Furthermore, as indicated above, the use of clamps 24 results in Wensink teaching away from a surface mount attachment to a connector board 26 component of a decapsulation machine 10. Consequently, the Examiner is prohibited from modification of Wensink, according to Zollo, to provide a surface mount of DUT 22 onto connector board 26, as required by Claim 13.

Therefore, Applicant respectfully submits that the Examiner fails to establish a *prima facie* obviousness rejection of Claim 13 over Wensink in view of Zollo. This failure is based on the Examiner's failure to establish that the combination of Wensink in view of Zollo teaches the receipt of an IC package installed onto a first surface of a PCB via surface mount attachment, as required by Claim 13. Instead of using a surface mount attachment, Wensink describes the use of clamps to temporarily affix DUT 22 to connector board 26 during decapsulation testing.

Consequently, for at least the reasons described above, Applicant respectfully submits that Claim 13, as amended, is patentable over the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 13.

Claims 14-16

Claims 14-16 depend from Claim 13 and, therefore, include the patentable claim features of Claim 13, as described above. Accordingly, Claims 14-16 are patentable over the references of record. Therefore, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 14-16.

CONCLUSION

In view of the foregoing, it is submitted that claims 9-16, as amended, patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No.

02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: April 24, 2003

By: _____
Joseph Lutz, Reg. No. 43,765

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office, Box AF, Assistant Commissioner for Patents, Washington, D.C. 20231, on April 24, 2003.

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Margaux Rodriguez *April 24, 2003*

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